Claim Listing

Please cancel claims 6-7, 11, 16, 18, 20, and 23-30.

1. (Currently Amended) A processing system ~~for providing a distributed directory based coherence protocol utilizing an associated memory having a coherence directory and associated directory data, the associated memory further~~ , comprising:

a memory comprising a coherence directory and associated coherence directory data, wherein the coherence directory comprises a plurality of memory blocks each [[associated with]] having different directory data;

a plurality of buffers interconnected to the memory;

a plurality of processing elements, each of the processing elements coupled to a different [[buffers]] one of the plurality of buffers;

wherein each of the processing elements comprises requesting means for requesting a selected one of the memory blocks from the memory;

wherein the memory comprises means [[associated with the memory,]] responsive to the requesting means [[for requesting for delivery]], ~~in response to the requesting,~~ for [[delivery of a corresponding]] providing the selected memory block ~~of the memory blocks, a corresponding set of~~ and the coherence directory data [[from the memory,]] corresponding to the selected memory block to [[an associated element]] a requesting one of the processing elements; and

wherein each of the processing elements comprises means [[for the processing elements]] for ~~detecting the delivery of the~~ receiving the selected memory block[[,]] and the coherence directory data corresponding to the selected memory block, and for determining if the selected memory block [[of the processing element]] is available for a particular access mode~~, and if not, performing coherence actions corresponding to the coherence directory data~~.

2. (Currently Amended) The system of Claim 1, wherein the memory blocks are configured to provide [[the]] a system memory [[space]].

3. (Currently Amended) The system of Claim 1, wherein the memory blocks are used to provide a level of cache in the system memory [[hierarchy]].

4. (Currently Amended) The system of Claim 1, wherein the processing elements are connected with the buffers [[connected to the memory]] via point to point links.

5. (Currently Amended) The system of Claim 1, wherein at least one of the processing elements [[contains]] comprises at least [[a first]] one processor, and [[at least]] another one of the processing elements [[contain]] comprises at least [[a second]] two processors.

6. (Canceled).

7. (Canceled).

8. (Currently Amended) The system of Claim 1, wherein [[memory requests]] a request by a processing element for one of the memory blocks from the memory [[resulting]] results in [[coherence actions]] an [[update]] updating of directory information to [[at least]] indicate a state ~~not corresponding to an indication of one of resident, shared, and exclusive states~~ requiring resolution.

9. (Currently Amended) The system of Claim 8, wherein the processing element[[s]] [[causing such at least one state]] issuing the request [[resolve them using]] also issues protocol requests.

10. (Currently Amended) The system of Claim 9, wherein [[other processors]] another processing element detecting the [[at least an on]] state [[and]] backs off and [[retry]] retries a request for the memory block at a later time~~, until the node having generated the at least one state, resolves the at least one state, by performing coherence actions and updating the coherence directory~~.

11. (Canceled).

12. (Currently Amended) A method for ~~implementing a distributed directory based coherence protocol~~ providing memory data to a requestor of the memory data, the method comprising:

requesting a memory block from a memory hierarchy level having a coherence directory and associated coherence directory data[[,]];

generating a response including the memory data and corresponding coherence directory data [[and updating directory information,]];

updating the coherence directory data corresponding to the memory data;

receiving [[a]] the response including the memory data and the corresponding coherence directory data from the memory hierarchy level[[,]];

~~a testing step to indicate~~ determining whether the received coherence directory data is compatible with a required access mode[[,]];

[[a step of]] performing at least one coherence action[[s]] if the ~~test indicates one of incompatibility or possible incompatibility~~ received coherence directory data is incompatible with the required access mode; and[[,]]

[[a step of]] providing the memory data to [[a]] the requestor of the memory data.

13. (Currently Amended) The method of Claim 12, wherein the [[requests and responses]] requesting of the memory block, and the generating and receiving of the response, are performed by sending and receiving data over [[logical]] point to point links.

14. (Currently Amended) The method of Claim 12, wherein the steps of generating [[a]] the response and updating the coherence directory [[information]] data are performed atomically [[with respect to other generating and updating steps]].

15. (Currently Amended) The method of Claim 12, wherein the coherence directory [[information]] data [[includes]] is indicative of a state [[indicating that]] wherein at least one node is performing at least one coherence action[[s]] as a result of receiving the response.

16. (Canceled).

17. (Currently Amended) The method of Claim 12, wherein the at least one coherence action[[s are performed by at least one]] involves a processing element [[by]] sending a coherence request[[s]] to another processing element[[s]].

18. (Canceled).

19. (Currently Amended) The method of Claim 12, wherein the response [[containing]] comprising the memory data and the corresponding coherence directory data is transmitted in a single response.

20. (Canceled).

21. (Currently Amended) The method of Claim 12, wherein the generating of the response is [[generated]] carried out under the control of a tag array.

22. (Currently Amended) The method of Claim 12, wherein the [[update]] updating of the coherence directory [[information]] data [[is limiting to]] involves the setting or resetting of a plurality of bits[[, in response to the requesting step]].

23. (Canceled).

24. (Canceled).

25. (Canceled).

26. (Canceled).

27. (Canceled).

28. (Canceled).

29. (Canceled).

30. (Canceled).